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Case Docket No. PHN 17,049

THE COMMISSIONER OF PATENTS AND TRADEMARKS, Washington, D.C. 20231

Enclosed for filing is the patent application of Inventor(s):
ANTONIUS H.M. HOLTSLAG

For: DISPLAYING VIDEO ON A PLASMA DISPLAY PANEL

ENCLOSED ARE:

[X] Appointment of Associates;
[X] Information Disclosure Statement, Form PTO-1449 and copies of documents listed therein;
[ ] Preliminary Amendment;
[X] Specification (10 Pages of Specification, Claims, & Abstract);
[X] Declaration and Power of Attorney:
(1 Page of a [X]fully executed [ ]unsigned Declaration);
[X] Drawing (4 sheet of [ ]informal [X]formal sheets);
[X] Certified copy of EUROPEAN application Serial No. 98202702.1;
[X] Authorization Pursuant to 37 CFR §1.136(a)(3)
[ ] Other: ;
[X] Assignment to U.S. PHILIPS CORPORATION.

FEE COMPUTATION

CLAIMS AS FILED				
FOR	NUMBER FILED	NUMBER EXTRA	RATE	BASIC FEE - $760.00
Total Claims	5 - 20 =	0	X $18 =	0.00
Independent Claims	3 - 3 =	0	X $78 =	0.00
Multiple Dependent Claims, if any			$260 =	0.00
TOTAL FILING FEE			=	$760.00

Please charge Deposit Account No. 14-1270 in the amount of the total filing fee indicated above, plus any deficiencies. The Commissioner is also hereby authorized to charge any other fees which may be required, except the issue fee, or credit any overpayment to Account No. 14-1270.

[ ]Amend the specification by inserting before the first line as a centered heading --Cross Reference to Related Applications--; and insert below that as a new paragraph --This is a continuation-in-part of application Serial No. , filed , which is herein incorporated by reference--.

CERTIFICATE OF EXPRESS MAILING

Express Mail Mailing Label No. EL215005285US **Date of Deposit** March 15, 1999 **I hereby certify that this paper and/or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.**

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Displaying video on a plasma display panel.

The invention relates to a method of displaying a video signal on a plasma display panel as defined in the precharacterizing part of claim 1. The invention further relates to a circuit for displaying a video signal on a plasma display panel as defined in the precharacterizing part of claim 4. The invention also relates to a plasma display device comprising a plasma display panel and a circuit for displaying a video signal on the plasma display panel as defined in the precharacterizing part of claim 5.

In a known Alternate Lighting In Surface Plasma Display Panel (further referred to as ALIS PDP) with n display lines, each display line comprises a plasma channel with which two spaced-apart select electrodes are aligned. Two consecutive plasma channels have one select electrode in common. The display lines are selected in an interlaced sequence so as to be able to select all display lines of this ALIS PDP one by one. First, during a first display field of display lines, the n/2 odd display lines are selected one by one, then, during a second display field of display lines, the n/2 even lines are selected one by one.

An interlaced video signal has a frame period with a first and a second video field period. Usually, the odd lines of the video signal form the first video field, and the even lines of the video signal form the second video field. When this interlaced video signal has to be displayed on the ALIS PDP, the odd lines of the video signal are displayed on the odd display lines, and the even lines of the video signal are displayed on the even display lines.

When a progressive video signal has to be displayed on the ALIS PDP, two approaches are known, dependent on the number of video lines to be displayed. When the number of video lines to be displayed is substantially equal to the number of display lines, the odd lines of the video signal are displayed on the odd display lines. Thus, the even lines of the video signal are not used, and the odd display lines are selected also in periods during which otherwise the even display lines would be selected. When the number of video lines is substantially equal to half the number of display lines, all the lines of the video signal are displayed on the odd display lines only.

In the situation where interlaced video (for example, HDTV) as well as progressive video (for example, SXGA) is displayed on the ALIS PDP, the display of the interlaced video becomes different for the odd and the even display lines.

It is, inter alia, an object of the invention to reduce the differences in the display of the odd and the even display lines.

To this end, a first aspect of the invention provides a method of displaying a video signal on a plasma display panel as claimed in claim 1. A second aspect of the invention provides a circuit for displaying a video signal on a plasma display panel as claimed in claim 4. A third aspect of the invention provides a plasma display with a circuit for displaying a video signal on the plasma display panel as claimed in claim 5. Advantageous embodiments are defined in the dependent claims.

The invention is based on the recognition that the display of progressive video on the odd display lines only, as performed in the prior art, causes the phosphors of the odd display lines to age at a faster rate than the phosphors of the even display lines. According to the invention, the progressive video is alternately displayed on the odd display lines only, or on the even display lines only. In both situations this is done during a certain period of time which is larger than a field period of the video signal. For example, the period of time is one hour. In this way, the phosphors of the odd and even display lines will age substantially equally and the artifacts during display of the interlaced video signal on all display lines decrease.

In an embodiment of the invention as claimed in claim 2, the number of video lines is smaller than or substantially equal to half the number of display lines. In this way, only a few or no video lines will not be displayed on the display lines.

In an embodiment of the invention as claimed in claim 3, the period of time during which the video signal is displayed on the odd or even lines only, is sufficiently large to prevent line flicker.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

In the drawings:

Fig. 1 shows part of the structure of a known progressively scanned PDP,

Fig. 2 shows part of the structure of the known ALIS PDP,

Fig. 3 shows a block diagram of a circuit for displaying a video signal on the known ALIS PDP, and

Figs. 4 A-D show voltages supplied to the select electrodes of the ALIS PDP to obtain an interlaced scan.

Fig. 1 shows part of the structure of a known progressively scanned PDP with n display lines D1,..., Dn. Each display line Di comprises a plasma channel Pi with which two spaced-apart select electrodes Si1, Si2 are aligned. A display line Di is selected to prime associated pixels Cij (see Fig. 3) by supplying a sufficiently high voltage between the two electrodes Si1, Si2. A line of black matrix material Bm separates two consecutive plasma channels Pi, Pi+1.

Because two select electrodes Si1, Si2 are associated with one plasma channel Pi only, it is possible to activate neighboring plasma channels Pi independently. This provides a progressive scan of the plasma channels Pi whereby the plasma channels Pi are activated successively one by one. Detailed information on such a PDP panel and the driving thereof can be found in EP-B-0549275, which is herein incorporated by reference.

Fig. 2 shows part of the structure of the known ALIS PDP. In the ALIS PDP with n display lines D1,..., Dn, each display line Di comprises a plasma channel Pi with which two spaced-apart select electrodes Si, Si+1 are aligned. Again, a display line Di is selected by supplying a sufficiently high voltage between the two electrodes Si, Si+1. Two consecutive plasma channels Pi, Pi+1have one electrode Si+1 in common. The display lines Di are selected in an interlaced sequence to provide a one-by-one selection of all display lines Di of this ALIS PDP. First, during a first field of display lines Di, the n/2 odd display lines Di are selected one by one, then, during a second field of display lines Di, the n/2 even display lines Di are selected one by one.

The addressing of the ALIS PDP is elucidated with respect to Fig. 3 and Figs. 4 A-D.

Fig. 3 shows a block diagram of a circuit for displaying a video signal Vs on the known ALIS PDP 1. The ALIS PDP 1 shown comprises plasma channels Pi extending in the horizontal direction. Two select electrodes Si, Si+1 are associated with each plasma channel Pi. Data electrodes Daj extend in the vertical direction. Overlapping regions of the plasma channels Pi and the data electrodes Daj form display cells or pixels Cij one of which is indicated by a circle.

It is known to generate the gray scales of the displayed video by driving the PDP in a sub-field mode. During each display field, a number of sub-fields is generated, each sub-field comprising a prime period and a sustain period. During the prime period, a select driver 2 selects the display lines (rows) Di one by one to prime the display cells Cij of the selected row Di with data signals Dsj. A data driver 3 which receives the video signal Vs supplies the data signals Dsj in parallel. During the sustain period, the select driver 2 supplies pulses to all the rows Di associated with the active display field. The plasma channels Pi are ignited a predetermined number of times to generate light from the pixels Cij primed to do so. The amount of light produced depends on the number of ignitions. Sustain periods with a different number of ignitions are associated with the different sub-fields in a display field period. The amount of light generated during a display field is the sum of the different amounts of light produced during the sub-fields of this display field. The PDP is able to produce gray scales because, during the priming period of each sub-field, it is possible to select whether a certain pixel has to produce light during the subsequent sustain period or not. Each sub-field may comprise an erase period, or the erase period may occur once in a display field. During the erase period, all pixels associated with the display field are erased. Detailed information on the sub-field operation of a PDP can be found in EP-B-0549275.

The timing circuit 4 receives the horizontal and vertical synchronization signals S of the video signal Vs to produce the timing signals for the select driver 2 and the data driver 3.

When a progressive video signal Vs has to be displayed on the ALIS PDP, two approaches are known, dependent on the number of video lines to be displayed. When the number of video lines to be displayed is substantially equal to the number of display lines Di, only the odd lines of the video signal Vs are displayed on only the odd display lines Di. Thus, the even lines of the video signal Vs are not displayed, and the odd display lines Di are selected also in periods during which otherwise the even display lines Di would be selected.

When the number of video lines is substantially equal to half the number of display lines Di, all the lines of the video signal Vs are displayed on the odd display lines Di only. The timing circuit 4 commands the select driver 2 to only select the lines of the odd field of display lines Di. The timing circuit 4 may receive information indicating the display mode, or the timing circuit 4 may detect the type of video signal Vs by evaluating the horizontal and vertical synchronization signal of the video signal Vs.

According to the invention, the progressive video Vs is displayed alternately on the odd display lines Di only, or on the even display lines Di only. In both situations, this is done during a certain period of time which is larger than a field period of the video signal Vs. For example, a certain period of time is one hour, or a certain period of time is related to the time the display is active. When the display is switched on to normal operation after it has been switched off or entered a standby mode, the video signal Vs is displayed on the other field of display lines Di. The timing circuit 4 may comprise a timer or a memory device, respectively, to generate the certain period in time. The timing circuit 4 commands the select driver 2 to only select the display lines Di of the odd field of display lines, or to only select the display lines Di of the even field of display lines.

Figs. 4 A-D show voltages supplied to the select electrodes Si of the ALIS PDP to obtain an interlaced scan. In all Figs. 4, voltages are denoted by a number 0, 1, -1, -2 to indicate the polarity and the relative value of the voltage concerned. For the sake of simplicity, an ALIS PDP with only a few select electrodes Si (S1 to S12), data electrodes Daj (Da1 to Da6) and display lines D1,...,D11 is shown. The voltages supplied to the odd select electrodes S1, S3, ..., S11 are shown to the left of the PDP. The even select electrodes S2, S4, ..., S12 are interconnected in two groups, the voltages supplied to these groups are shown to the right of the PDP. The data voltages Dsj are shown below the PDP. In a selected display line Di, Pixels Cij which are primed to generate light are indicated by a solid circle, pixels Cij which are primed to not produce light are indicated by a dashed circle.

Fig. 4A shows the voltages to select display line D4 during a certain display field. Fig. 4B shows the voltages to select display line D6 during the same display field. Fig. 4C shows the voltages to select display line D5 during a succeeding display field, and Fig. 4D shows the voltages to select display line D7 during this succeeding field.

It is possible to select the display lines Di of a certain display field in different ways. As an example, this is explained with respect to Figs. 4A and 4B. All even rows D2, D4,...,D10 may be selected one by one by first selecting a certain row, let us assume D4, in accordance with Fig. 4A. Next, the consecutive even row D6 is selected as shown in Fig. 4B. Then, the even row D8 is selected in accordance with Fig. 4A by applying a –1 voltage to select electrode S5 and a –2 voltage to select electrode S9. Next, the even row D10 is selected in accordance with Fig. 4B by applying a –1 voltage to select electrode S7 and a –2 voltage to the select electrode S11. And so on. This selection scheme has the disadvantage that the voltages on the even select electrodes have to change for every display line Di, which causes a large dissipation. This drawback is prevented by first selecting the rows D4, D8 in accordance with Fig. 4A and next the rows D2, D6, D10 in accordance with Fig. 4B. In the same way, it is possible to select the odd display rows Di first in accordance with Fig. 4C and next in accordance with Fig 4D.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The embodiments describe an ALIS PDP with plasma channels extending in the horizontal direction. Alternatively, the PDP may be rotated through 90°, such that the plasma channels extend in the vertical direction. The plasma channels may be open towards each other, such that a layer of plasma exists. Instead of plasma channels, the PDP may comprise plasma cells.

An aspect of the invention is defined in a method of displaying a video signal Vs with m video lines in a video field period on a plasma display panel 1 having n display lines Di. The n display lines Di are selected (2) in an interlaced way to subsequently select a first and a second field of n/2 display lines Di to display an interlaced video signal Vs. For displaying a progressive video signal Vs, the m video lines are alternately displayed (3) on the first field of display lines Di only, or on the second field of display lines Di only, both during respective time periods which are longer than the video field period.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of other elements or steps than those listed in a claim. The invention can be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware.

CLAIMS:

1. A method of displaying a video signal (Vs) with video lines in a video field period on a plasma display panel (1) having a first and a second display field of display lines, the display lines (Di) of the first display field being in an interlaced position with respect to the display lines (Di) of the second display field, the method comprising the steps of:

alternately selecting (2) several times the first display field only, or the second display field only, both during respective time periods which are longer than the video field period, and

supplying (3) video data signals (Dsj) in conformance with the video lines to the display lines (Di) of the selected display field.

2. A method as claimed in claim 1, characterized in that the number of video lines in a video field period is smaller than or substantially equal to the number of display lines (Di) of the first or second display field.

3. A method as claimed in claim 1, characterized in that the time periods are substantially longer than the video field period.

4. A circuit for displaying a video signal (Vs) with video lines in a video field period on a plasma display panel (1) having a first and a second display field of display lines, the display lines (Di) of the first display field being in an interlaced position with respect to the display lines (Di) of the second display field, the circuit comprising:

means (2) for alternately selecting several times the first display field only, or the second display field only, both during respective time periods which are longer than the video field period, and

means (3) for supplying video data signals (Dsj) in conformance with the video lines to the display lines (Di) of the selected display field.

5. A plasma display device comprising a plasma display panel (1) and a circuit for displaying a video signal (Vs) with video lines in a video field period on a plasma display panel (1) having a first and a second display field of display lines, the display lines (Di) of the first display field being in an interlaced position with respect to the display lines (Di) of the second display field, the circuit comprising:

means (2) for alternately selecting several times the first display field only, or the second display field only, both during respective time periods which are longer than the video field period, and

means (3) for supplying video data signals (Dsj) in conformance with the video lines to display lines (Di) of the selected display field.

ABSTRACT:

A method of displaying a video signal (Vs) with m video lines in a video field period on a plasma display panel (1) which has n display lines (Di) is described. The n display lines (Di) are selected (2) in an interlaced way to subsequently select a first and a second field of n/2 display lines (Di) to display an interlaced video signal (Vs). For displaying a progressive video signal (Vs), the m video lines are alternately displayed (3) on the first field of display lines (Di) only, or on the second field of display lines (Di) only, both during respective time periods which are longer than the video field period.

(Fig. 3)

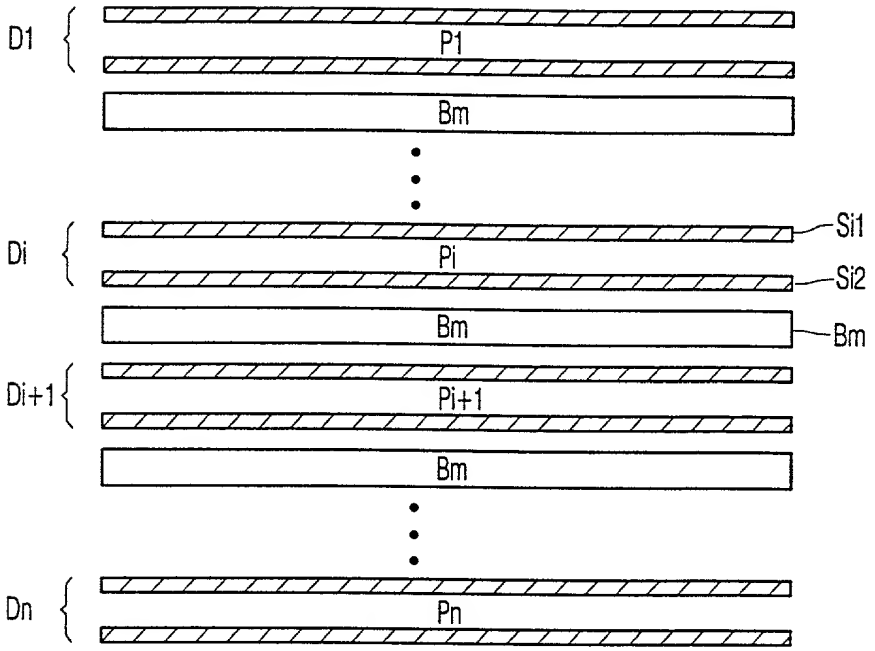
D1
P1
Bm
Di
Si1
Pi
Si2
Bm
Bm
Di+1
Pi+1
Bm
Dn
Pn

FIG. 1

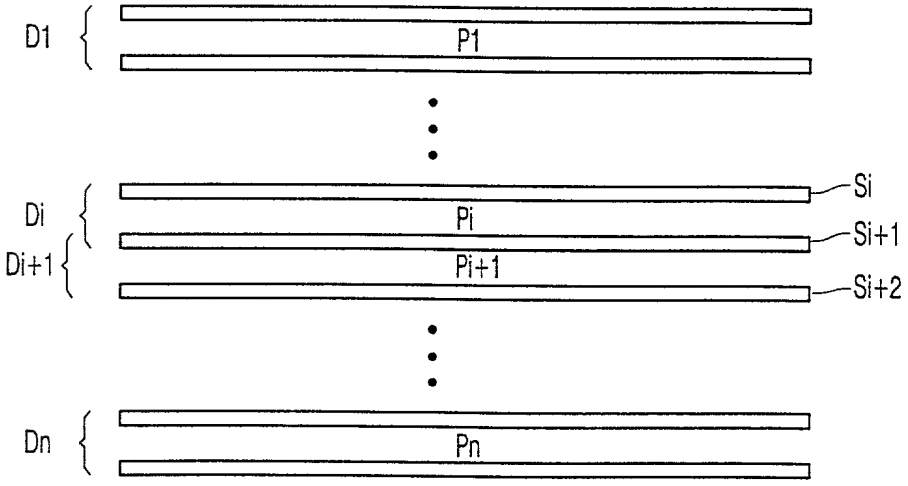
D1
P1
Si
Di
Pi
Si+1
Di+1
Pi+1
Si+2
Dn
Pn

FIG. 2

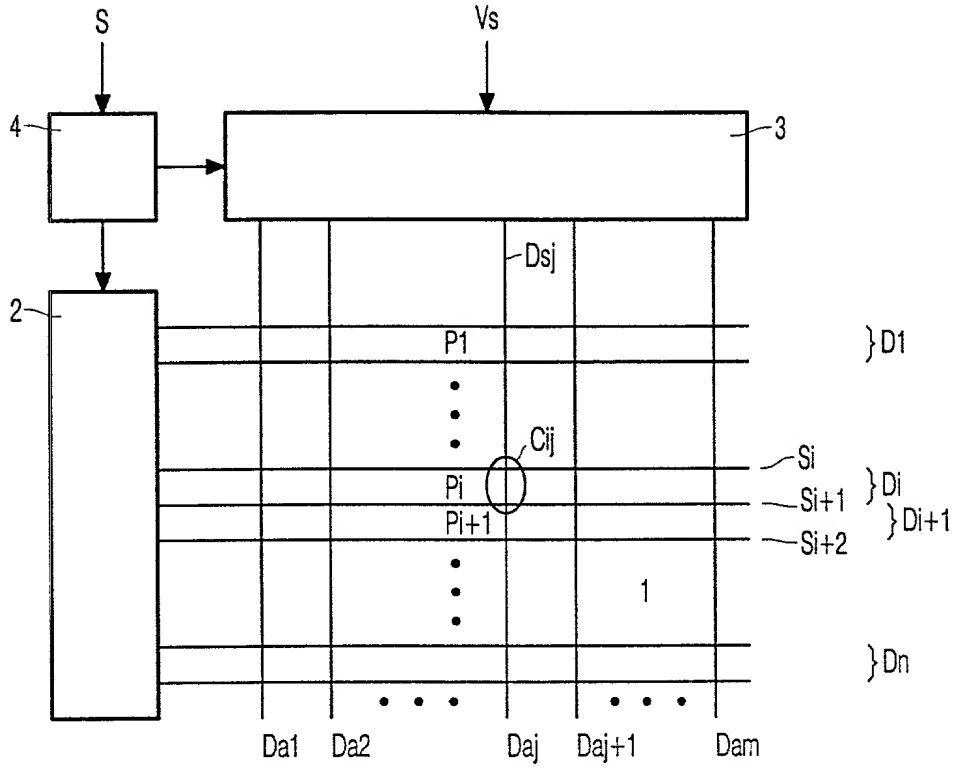
S
Vs
4
3
2
Dsj
P1
D1
Cij
Si
Pi
Si+1
Di
Pi+1
Si+2
Di+1
1
Dn
Da1
Da2
Daj
Daj+1
Dam

FIG. 3

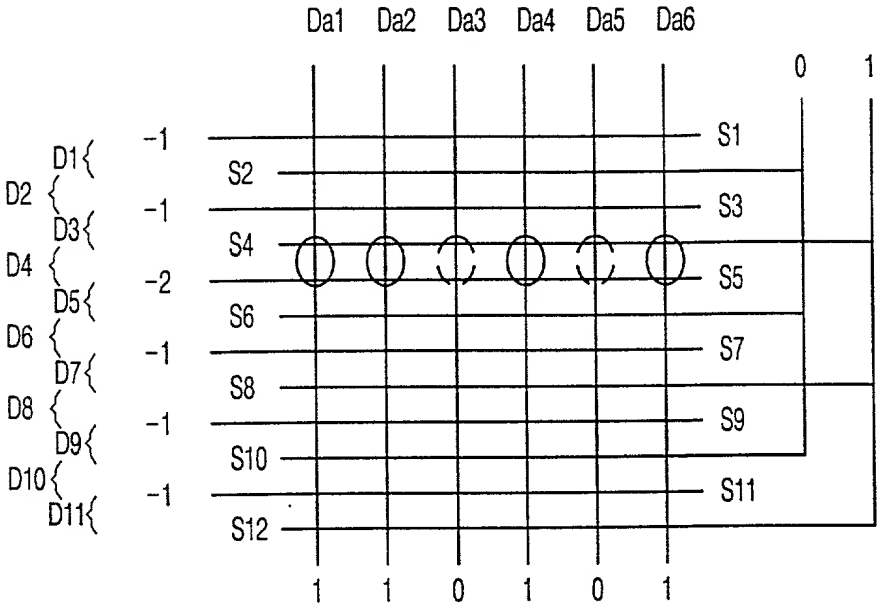
Da1
Da2
Da3
Da4
Da5
Da6
0
1
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
-1
-1
-2
-1
-1
-1
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
1
1
0
1
0
1

FIG. 4A

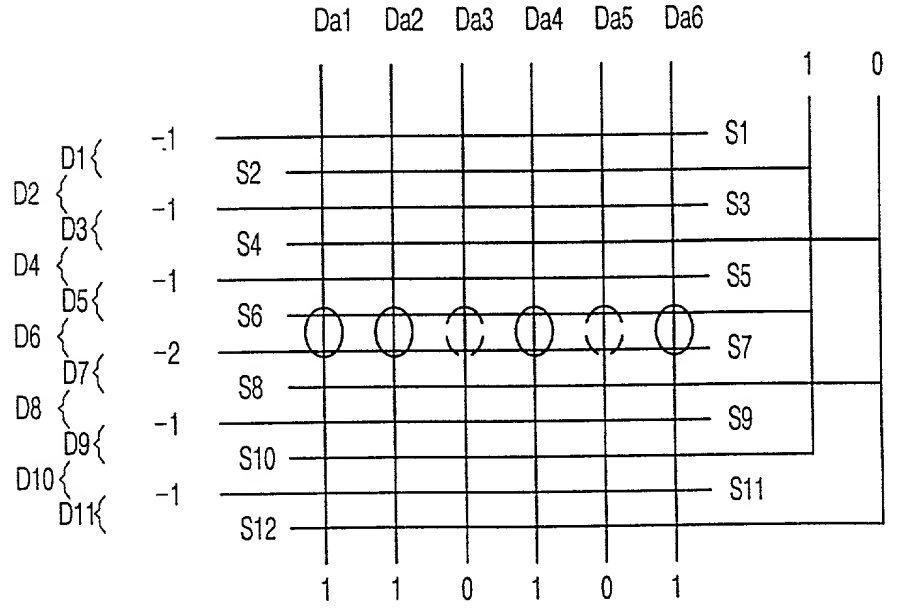
Da1
Da2
Da3
Da4
Da5
Da6
1
0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
-1
-1
-1
-2
-1
-1
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
1
1
0
1
0
1

FIG. 4B

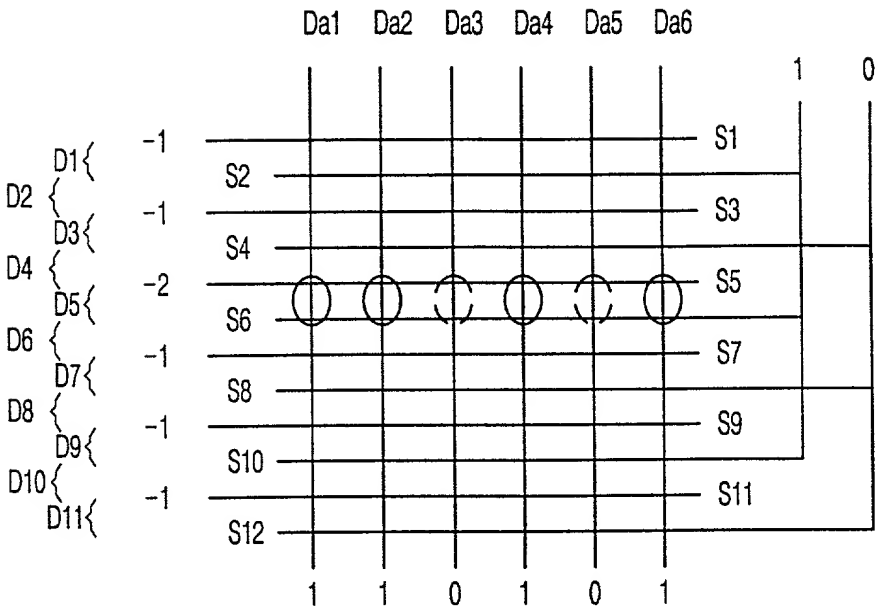
Da1 Da2 Da3 Da4 Da5 Da6
1 0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
-1
-1
-2
-1
-1
-1
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
1 1 0 1 0 1

FIG. 4C

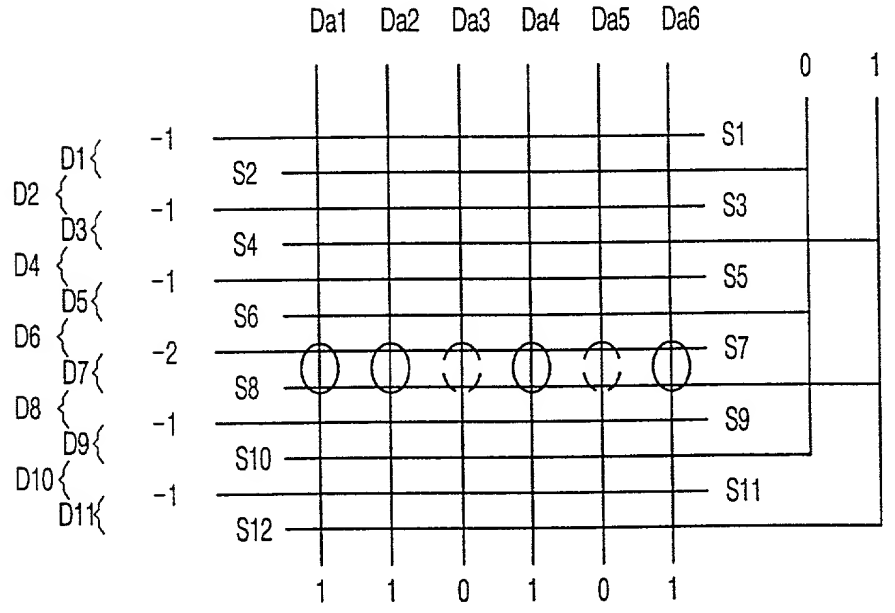
Da1 Da2 Da3 Da4 Da5 Da6
0 1
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
-1
-1
-1
-2
-1
-1
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
1 1 0 1 0 1

FIG. 4D

DECLARATION and POWER OF ATTORNEY

ATTORNEY'S DOCKET NO.:
PHN 17.049

As a below named inventor, I hereby declare that:
My residence, post office address and citizenship are as stated below next to my name.
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
"Displaying video on a plasma display panel"
the specification of which (check one)
☒ is attached hereto.
☐ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by the amendment(s) referred to above.
I acknowledge the duty to disclose information which is material to patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).
I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

COUNTRY	APP.NUMBER	DATE OF FILING (DATE,MONTH, YEAR)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
Europe	**98202702.1**	**12 August 1998**	**YES**

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1,56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

PRIOR UNITED STATES APPLICATION(S)

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (PATENTED, PENDING, ABANDONED)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Algy Tamoshunas, Reg. No. 27,677
Jack E. Haken, Reg. No. 26,902

SEND CORRESPONDENCE TO: Corporate Patent Counsel; U.S. Philips Corporation; 580 White Plains Road; Tarrytown, NY 10591	DIRECT TELEPHONE CALLS TO: (name and telephone No.) (914) 332-0222

Dated: February 18, 1999		Inventor's Signature: Ton Holtslag		
Full Name of Inventor	Last Name **HOLTSLAG**	First Name **Antonius**	Middle Name **H.M.**	
Residence & Citizenship	City **Eindhoven**	State or Foreign Country **The Netherlands**	Country of Citizenship **The Netherlands**	
Post Office Address	Street **Prof.Holstlaan 6**	City **5656 AA Eindhoven**	State or Country **The Netherlands**	Zip Code
Dated:		Inventor's Signature:		
Full Name of Inventor	Last Name	First Name	Middle Name	
Residence & Citizenship	City	State or Foreign Country	Country of Citizenship	
Post Office Address	Street	City	State or Country	Zip Code

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of
ANTONIUS H.M. HOLTSLAG

Atty. Docket
PHN 17,049

Serial No.

Group Art Unit

Filed: CONCURRENTLY

Examiner:

Title: DISPLAYING VIDEO ON A PLASMA DISPLAY PANEL

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

APPOINTMENT OF ASSOCIATES

Sir:

The undersigned Attorney of Record hereby revokes all prior appointments (if any) of Associate Attorney(s) or Agent(s) in the above-captioned case and appoints:

EDWARD W. GOODMAN **(Registration No. 28,613)**

c/o U.S. PHILIPS CORPORATION, Intellectual Property Department, 580 White Plains Road, Tarrytown, New York 10591, his Associate Attorney(s)/Agent(s) with all the usual powers to prosecute the above-identified application and any division or continuation thereof, to make alterations and amendments therein, and to transact all business in the Patent and Trademark Office connected therewith.

ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND THE LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE UNDERSIGNED ATTORNEY OF RECORD.

Respectfully,

Algy Tamoshunas, Reg. 27,677
Attorney of Record

Dated at Tarrytown, New York
this 15TH day of March, 1999.

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